

THE INVENTION CLAIMED IS:

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

5 forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and on the gate;

forming trenches in the semiconductor substrate around the gate;

forming an interlayer dielectric above the semiconductor substrate; and

10 forming contacts in the interlayer dielectric to the silicide.

2. The method as claimed in claim 1 wherein forming the trenches further comprises:

forming a sidewall spacer around the gate;

forming a cusp at the outer edge of the sidewall spacer;

15 removing the sidewall spacer at the cusp; and

forming the trenches at the outer edge of the sidewall spacer.

3. The method as claimed in claim 1 wherein:

forming the trenches uses an etching process that etches the semiconductor substrate.

4. The method as claimed in claim 1 wherein:

20 forming the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

5. The method as claimed in claim 1 wherein:

25 forming the contacts to the silicide uses materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

30 forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and on the gate
forming a sidewall spacer around the gate;
forming trenches in the semiconductor substrate at the outer edges of the sidewall
spacer;
5 forming an interlayer dielectric above the semiconductor substrate; and
forming contacts in the interlayer dielectric to the silicide.

7. The method as claimed in claim 1 wherein forming the sidewall spacer further
comprises:

forming an insulating liner around the gate; and
10 forming an insulating film having a cusp over the insulating liner.

8. The method as claimed in claim 1 wherein:
forming the trenches uses an etching process that etches the semiconductor substrate

9. The method as claimed in claim 1 wherein:
forming the interlayer dielectric deposits a dielectric material having a dielectric
15 constant selected from a group consisting of medium, low, and ultra-low
dielectric constants.

10. The method as claimed in claim 1 wherein:
forming the contacts to the ultra-uniform silicide uses materials selected from a group
consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy
20 thereof, a compound thereof, and a combination thereof.

11. An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
25 source/drain junctions in the semiconductor substrate;
a silicide on the source/drain junctions and on the gate;
trenches in the semiconductor substrate around the gate;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.

30 12. The integrated circuit as claimed in claim 11 wherein the trenches further
comprise:

a sidewall spacer around the gate, wherein the trenches are at the outer edge of the sidewall spacer.

13. The integrated circuit as claimed in claim 11 wherein:
the trenches extend into the semiconductor substrate to a level lower than the silicide.

5 14. The integrated circuit as claimed in claim 11 wherein:
the interlayer dielectric comprises a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

10 15. The integrated circuit as claimed in claim 11 wherein:
the contacts to the silicide comprises materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

16. An integrated circuit comprising:
a semiconductor substrate;
15 a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
source/drain junctions in the semiconductor substrate;
a silicide on the source/drain junctions and on the gate
a sidewall spacer around the gate;
20 trenches in the semiconductor substrate at the outer edges of the sidewall spacer;
an interlayer dielectric above the semiconductor substrate; and
contacts in the interlayer dielectric to the silicide.

17. The integrated circuit as claimed in claim 16 wherein the sidewall spacer further comprises:

25 an insulating liner around the gate; and
an insulating film over the insulating liner.

18. The integrated circuit as claimed in claim 16 wherein:
the trenches extend into the semiconductor substrate to a level lower than the silicide.

19. The integrated circuit as claimed in claim 16 wherein:

the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

20. The integrated circuit as claimed in claim 16 wherein:

5 the contacts to the silicide comprise materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.